AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A reconfigurable control structure for CPUs, comprising:

a first control unit with a first instruction set of basic instructions associated therewith, wherein the first control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in the first instruction set;

a second control unit, with a second instruction set of selectively modifiable instructions associated therewith, wherein the second control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in the second instruction set;

a programming element associated with said second control unit for rendering said second instruction set selectively modifiable;

at least one circuit element for supplying instruction codes to be executed to said first control unit and to said second control unit, so that each instruction can be executed under the control of at least one between said first control unit and said second control unit according to whether each instruction is comprised within at least one between said first instruction set and said second instruction set, wherein the at least one circuit element is configured for sending the instruction codes to be executed in an undifferentiated way to the first control unit and the second control unit;

a selector module configured for recognizing whether the instruction to be executed each time supplied by the at least one circuit element belongs to the first instruction set or to the second instruction set, wherein the control units have respective state outputs for outputting state information and respective state inputs for receiving state information;

a single state register having an output connected to the state inputs of the control units; and

a multiplexer having first and second inputs coupled respectively to the state outputs of the control units, the multiplexer driven by the selector module and configured for sending the state register a state signal identifying which of the first and second control units generates the control signals for the instructions to be executed.

2. (Cancelled)

3. (Previously Presented) The structure according to claim 1, further comprising an output module which has:

a first set of input lines connected to an output of said first control unit;

a second set of input lines connected to an output of said second control unit; and

a set of output lines;

wherein said output module is connected to said selector module for transferring on said set of output lines the signal present on said first set of input lines and on said second set of input lines when said selector module recognizes whether the instruction processed each time by the structure belongs to said first instruction set or to said second instruction set.

4. (Cancelled)

5. (Original) The structure according to claim 1 wherein said first control unit is configured as a wired-logic control unit.

6. (Cancelled)

7. (Original) The structure according to claim 1 wherein said second control unit is basically configured as a microprogrammed-logic control unit.

8. (Previously Presented) The structure according to claim 1, wherein said second control unit is configured as a finite state machine with a memory associated therewith which is able to receive a stored microprogram defining the sequences of the control signals of said finite state machine.

9. (Original) The structure according to claim 1 wherein said first control unit and said second control unit are configured as finite state machines having respective numbers of state bits and the number of state bits of said second control unit is greater than or equal to the number of state bits of said first control unit.

10. (Original) The structure according to claim 1, wherein:

said first control unit is of a hardwired type; and

said second control unit is programmable, programming of said second control unit being carried out by said first control unit by means of instructions.

11. (Original) The structure according to claim 10, wherein programming of said second control unit by said first control unit is carried out by means of an operation of memory programming.

12. (Previously Presented) The structure according to claim 10 wherein programming of said second control unit by said first control unit is carried out by means of at least one programming instruction included in said first instruction set.

13-16. (Cancelled)

17. (Previously Presented) A reconfigurable control structure for CPUs, comprising:

an input for receiving instructions;

an output for presenting control signals produced by execution of the instructions;

a hard-wired control unit coupled between the input and the output and structured to execute a pre-defined set of the instructions into a plurality of the control signals, wherein the hard-wired control unit includes a finite state machine that is able to assume an inoperative state and at least one active state for execution of the instructions of the pre-defined set;

a programmable control unit coupled between the input and the output and structured to execute a programmable set of the instructions, the programmable control unit including a memory that stores definitions of the programmable set of instructions and an execution unit that executes the instructions according to the stored definitions to produce a plurality of the control signals, wherein the programmable control unit includes a finite state machine that is able to assume an inoperative state and at least one active state for execution of the instructions of the programmable set;

a selector module coupled to the input and configured to recognize whether each of the instructions received at the input is to be executed by the hard-wired control unit or by the programmable control unit, wherein the control units have respective state outputs for outputting state information and respective state inputs for receiving state information;

a switching device having first and second inputs coupled respectively to the state outputs of the control units, an output, and a control input coupled to an output of the selector module, the switching device being structured to selectively connect the output of the switching device to one of the first and second inputs depending on which of the control units the selector module recognizes as being appropriate for executing a current one of the instructions received by the selector module; and

a state register having an input connected to the output of the switching device and an output connected to the state inputs of the control units.

18. (Cancelled)

19. (Previously Presented) The control structure of claim 17, further comprising:

an output module having a first input connected to an output of the hard-wired control unit, a second input connected to an output of the programmable control unit, an output coupled to the output of the control structure, and a control input coupled to an output of the selector module, the output module being structured to selectively connect the output of the output module to one of the first and second inputs depending which of the control units the selector module recognizes as being appropriate for executing a current one of the instructions received by the selector module.

20-22. (Cancelled)

23. (Original) The control structure of claim 17 wherein programming of the programmable control unit by the hard-wired control unit is carried out by means of at least one programming instruction included in the pre-defined set of instructions.

24. (Currently Amended) A reconfigurable control structure for CPUs, comprising:

a hard-wired control unit with a first instruction set of basic instructions associated therewith, wherein the hard-wired control unit is configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in the first instruction set;

a programmable control unit configured as a finite state machine that is able to assume an inoperative state and at least one active state for execution of a respective instruction comprised in a second instruction set of selectively modifiable instructions associated therewith, wherein the programmable control unit is programmed by the hard-wired control unit by means of at least one basic instruction within the first instruction set;

at least one circuit element for supplying instruction codes to be executed to said hard-wired control unit and to said programmable control unit, so that each instruction can be executed under the control of at least one between said hard-wired control unit and said programmable control unit according to whether each instruction is comprised within at least one between said first instruction set and said second instruction set, wherein the at least one circuit element is configured for sending the instruction codes to be executed in an undifferentiated way to the hard-wired control unit and the programmable control unit;

a selector module configured for recognizing whether the instruction to be executed each time supplied by the at least one circuit element belongs to the first instruction set or to the second instruction set, wherein the control units have respective state outputs for outputting state information and respective state inputs for receiving state information;

a single state register having an output connected to the state inputs of the control units; and

a multiplexer having first and second inputs coupled respectively to the state outputs of the control units, the multiplexer driven by the selector module and configured for sending the state register a state signal identifying which of the hard-wired and programmable control units generates the control signals for the instructions to be executed.

25. (Previously Presented) The structure according to claim 24, wherein programming of said programmable control unit by said hard-wired control unit is carried out by means of an operation of memory programming.

26. (Previously Presented) The structure according to claim 24, further comprising an output module comprising:

a first set of input lines connected to an output of said hard-wired control unit;

a second set of input lines connected to an output of said programmable control unit; and

a set of output lines;

wherein said output module is connected to said selector module for transferring on said set of output lines the signal present on said first set of input lines and on said second set of input lines when said selector module recognizes whether the instruction processed each time by the structure belongs to said first instruction set or to said second instruction set.

27. (Previously Presented) The structure according to claim 24 wherein said programmable control unit is basically configured as a microprogrammed-logic control unit.

28. (Previously Presented) The structure according to claim 27, wherein said programmable control unit is configured as a finite state machine with a memory associated therewith which is able to receive a stored microprogram defining the sequences of the control signals of said finite state machine.

29. (Previously Presented) The structure according to claim 24 wherein said hard-wired control unit and said programmable control unit are configured as finite state machines having respective numbers of state bits and the number of state bits of said programmable control unit is greater than or equal to the number of state bits of said hard-wired control unit.